SONOMA STATE UNIVERSITY | ENGINEERING

EE 210L

1. **Course Number & Name:** EE 210L, Digital Circuit and Logic Design Lab
2. **Course Credit and Contact hours:** 1 Unit, 3 hours Lab
3. **Course Coordinator:** Dr. Sudhir Shrestha
4. **Textbook:** Morris R. Mano and Michael D. Ciletti, *Logic Design*, 5th ed., Pearson, 2012, ISBN 13: 978-0132774208
5. **Supplemental Materials:** Lab instructions and Slides and access to Verilog Server are provided in the lab
6. **Specific Course Information:**
   a. **Description:** Hands-on experience for logic gates, combinatorial logic, analysis and design of combinatorial circuits, electronic circuits for various logic gates, flip-flops, registers, and counters, sequential circuits and state machines. This course fulfills GE A3
   b. **Prerequisites:** EE 112, or consent of instructor
   c. **Co-Requisite:** EE 230, or consent of instructor
   d. **Status:** ☒ Required for EE program, ☐ Elective, ☐ Selected Elective
7. **Specific Goals for the Course:**
   a. **Specific outcomes of instruction:** Upon successful completion of this course the students will be able to:
      i. Learn and practice the Verilog High Description Language.
      ii. Design, connect, and test various combinational circuits using logical gates.
      iii. Simulate and test various combinational circuits using Verilog.
      iv. Design, connect, and test various sequential circuits using flip-flops.
      v. Simulate and test various sequential circuits using Verilog.
   b. **This course supports the following ABET Student Outcomes:**
      i. SO-6: an ability to develop and conduct appropriate experimentation, analyze and interpret data, and use engineering judgment to draw conclusions.
8. **Brief List of Topics and Experiments to be Covered in the Lab:**
   a. Intro to Multisim

b. Binary to decimal conversion with summing amplifier

c. Combination of logical gates
d. Intro to Linux
e. Intro to Verilog
f. EX_OR, EX_NOR and Verilog
g. Troubleshooting of digital circuits
h. Half-adder and full-adder and Verilog
i. Combinational circuit design procedure with example
j. Encoder and decoder, Verilog
k. Multiplexer / demultiplexer, Verilog
l. Flip-flop and Verilog
m. Ripple counter
n. Synchronous binary counter
o. Sequential circuit design procedure with example
p. Logical lock project using sequential logic